SPM Instruction Manual.

The Near Field Interaction Microscope (NEFION) system is an implementation of a multipurpose Scanning Probe Microscope with scanning and spectroscopy capabilities.

The main parts of the system are,

**The PLL Nanonis Module.**

**FPGA Card (inside PC).**

**FPGA Breakout box.**

**Set of sensors.**

**Set of preamplifiers.**

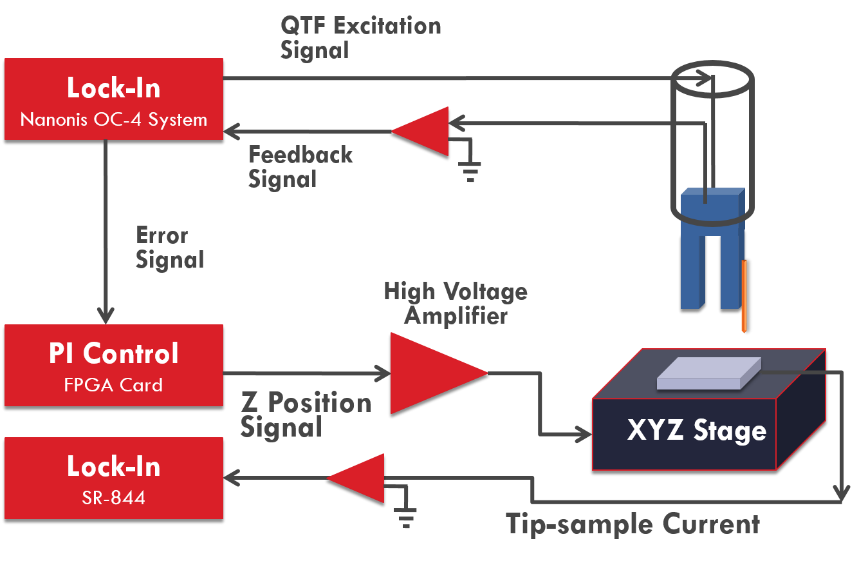
**Set of Cables.**

**Mad city Labs piezo stages.**

**Mad City Labs Piezo Controllers.**

**Sofware control for Scanning and Spectroscopy.**

In Part 1 We will start with the description of these parts and learn about their characteristics. Latter in Part 2 we will see how they work together and form the entire SPM / Approach and Retract System. Part 3 will show the procedure to start the system and how to operate it in its different modes. Part 4 will show a few examples of the results you can obtain at the end of each experiment.



**PART 1**

**DESCRIPTION OF THE MAIN PARTS.**

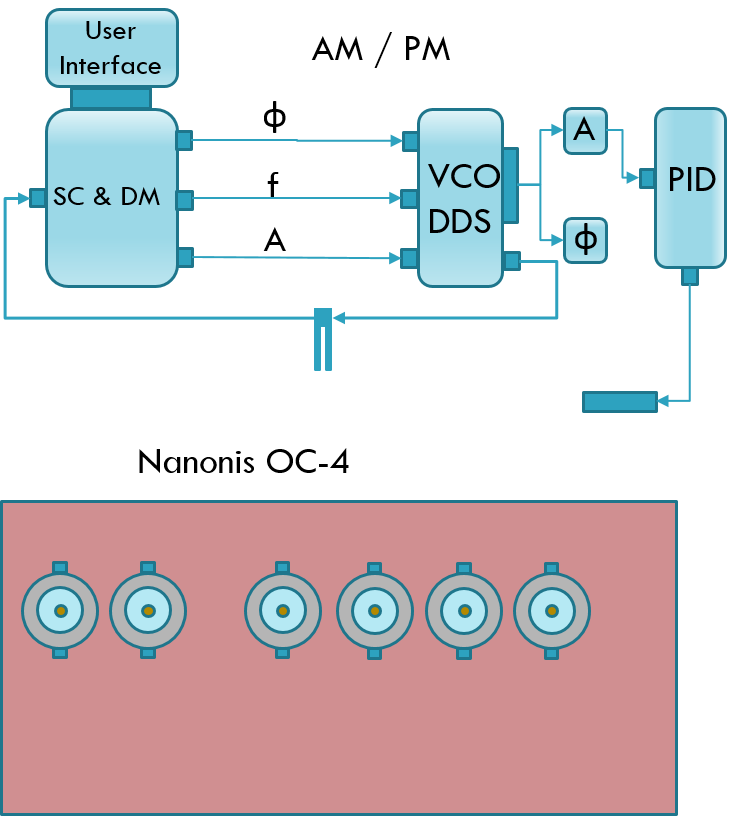
**The PLL Nanonis Module.**

The PLL is a unique part of the system. Is the part of the measurement equipment that transforms the treated signal from a voltage representing the amplitude of the sensors motion (in the form of a quasi-sinusoidal wave) to values of amplitude, phase and frequency shift (with respect to an excitation signal produced by the same PLL).

It needs to be integrated with all other parts. This is done through its BNC input and outputs. The datasheet can be found at <http://www.specs-zurich.com/upload/cms/user/OC4ProductBrochure.pdf>.

The PLL has an input BNC connector, an output BN connector (excitation signal), and outputs for the amplitude, phase, frequency shift and two auxiliary outputs, of which only one (AUX 1) can be used by the operator in normal operation procedure.

Figure 1 shows the connections from the PLL to the FPGA breakout box.



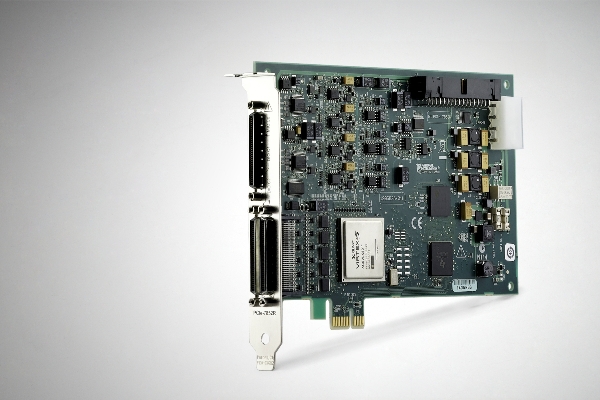
What is SC, DM, DDS? [Spell them out)

Fig #. Detailed components (top) inside the Nanonis OC-4 unit for performing SPM frequency modulation.

**The FPGA Card**

The FPGA is the acronym for the Field-Programmable Gate Array. It means exactly what the name implies. It is an arrangement of digital gates (NAND’s, NOR’s) that can be rearranged (programmed) by applying electric fields, which means that you create circuits without physically changing the circuit. (? Expression no clear] This provides a flexible environment for creating circuits to perform tasks that would take too much time for a PC to perform. As an example, consider the latency time of a normal PC running Windows, which is about 2 ms. And it is not clocked, which means that it will not perform any given operation within a time frame set by a clock [explain this better; no clear]. It will read a measurement as soon as it can (because it performs several actions in the background) and has a list of priorities. This is not a situation you want to have when trying to control in real time the distance between a tip and sample that are a few nanometers away from each other. In contrast, the FPGA can make operations as fast as every 45 nanoseconds period. In reality the time it takes to react to an input signal is limited by the time it takes an Analog to Digital converter (ADC) to convert the analog signal to a digital signal and vice versa. With a rate of 750 kSamples/second at the input and 1 Msamples/second at the output, the current time for the PCIe-7852 card is 1.33+1=2.33 μseconds [how do you get this number?], which is appropriate for the purpose of controlling the tip-sample-distance.

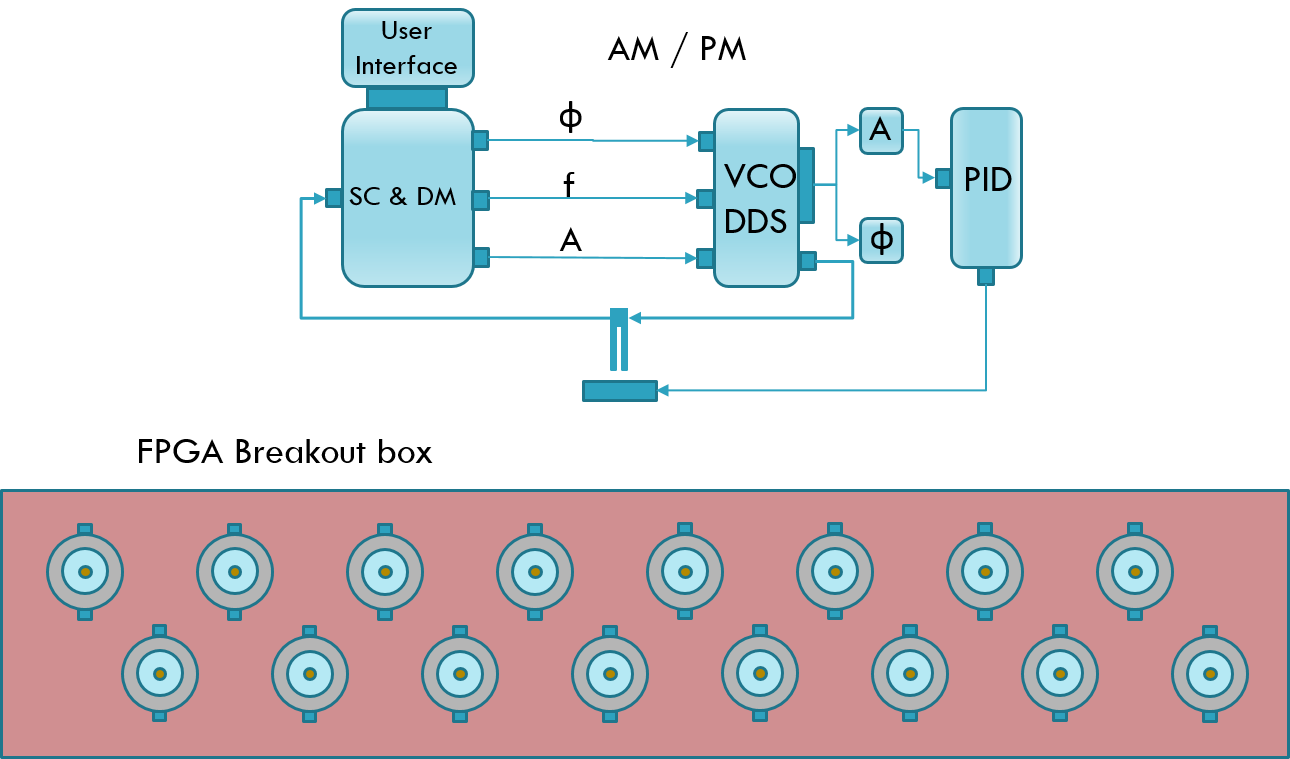
The FPGA card is programmed with Labview. The way the GUI works is explained in PART 3 of this manual. Here we will explain how the card performs its tasks.

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**The FPGA breakout box.**

The FPGA breakout box is connected to the actual FPGA, which is located inside the PC through a special National Instruments (NI) cable. The purpose of this box is to provide easy communication between the FPGA card and the external world. It has analog inputs and outputs (I/O), and some digital I/O’s as well.

In essence this breakout box is the front panel of the FPGA and the core of the system. All of the measurements and error signals converge here and all of the command signals (the signals that drive the motion of the piezostages) are delivered from this breakout box. The reason is that the FPGA contains the software that calculates the PID alghorithm, processes the data that forms the images and traces, calculates the signals from the sensors for easy reading, etc. The most time intensive calculations are performed in the actual card, while the Graphic user interfece (GUI) is run on the PC’s processor.



**The High Resolution Stage.**

The High resolution stage (HRS) is the solution that we found for the shortcoming in implementing PID lock-in, which consists in not having enough precision to guarantee position control in the order of nanometers. The strategy consisted of using two signals: one used as a coarse motion and the other as a fine motion. Both signals where added with the HRS external implementation. The internal implementation implied the modification and an increase in complexity of the PI alghorithm. The result of the internal implementation is summarized in Figure 3.

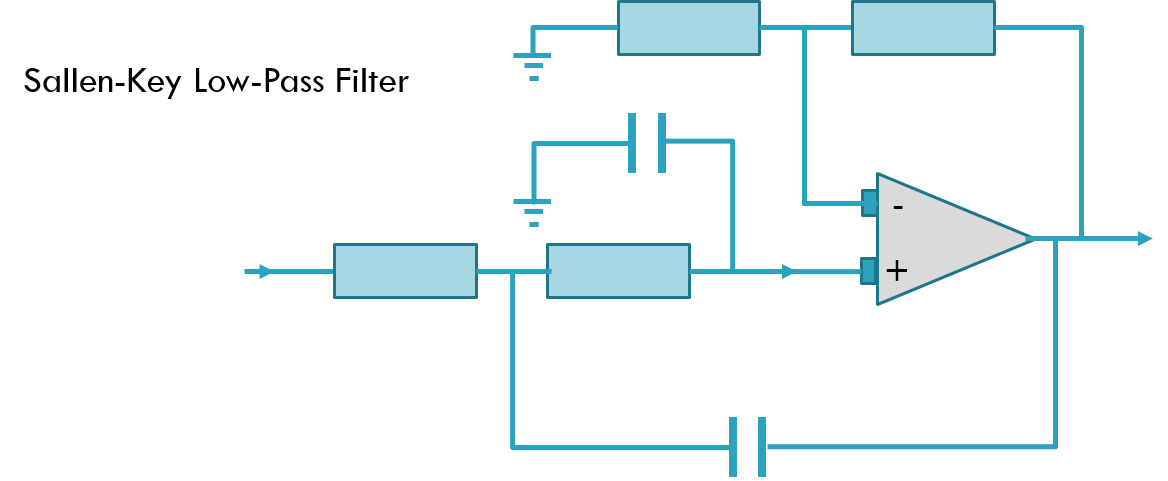


**The Preamplfiers.**

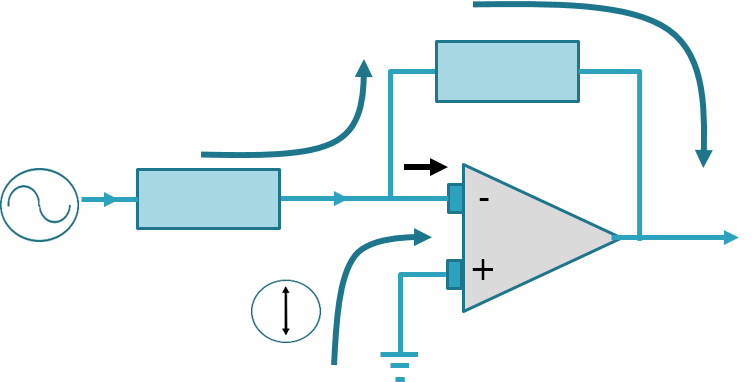
The preamplifiers and filters perform the signal conditioning of the measured signals. What does this mean?. It means that it throws away any component of the signal that does not fall in the frequency range we are working with. This is done by proper analog circuitry. The main components are filters and the type fo filters used in this project are active filters. In general active filters are the better choice when it comes to low frequency (lower than 1 GHz) signals. Active filters require les components and have the advantage of having high or low impedance at the input and low impedance at the output, which is useful for many applications. They use operational amplifiers and need a source of power as a consequence. Despite the fact the lock in amplifier has an intrinsic noise rejection arquitechture, wide band noise is still important and the main application occurs when we work with the FPGA input and outputs.

The main reason comes from the signal conditioning at the FPGA breakout box. The breakout box provides some shielding from noise sources, but does not filter or treats the signal in any other way. If the signals are to be sent to the FPGA, signal conditioning needs to be done. As a first approach (an easy implementation if the FPGA has enough resources) a digital filter can be implemented for inputs. The same solution cannot be applied to outputs though, since the noise is introduced outside of the FPGA. Most importantly, the signals that control the Piezo stages need to be as clean as possible. A quick calculation portrays the signal level needed for a precise control in the subnanometer regime.

The active filter diagram used for our filters is shown below.



The design of the filters can take from a few days to several weeks. The main problem consist in knowing the particular environment, connections that you are going to be facing. Specially if you are not trained in Electronic Engineering. However, every good scientist should be able to at least implement a basic design to meet the needs of a particular project. Depending on the budget (you can always buy a commercial low noise amplifier) a decent device in terms of noise and amplification can be obtained.



**PART 2**

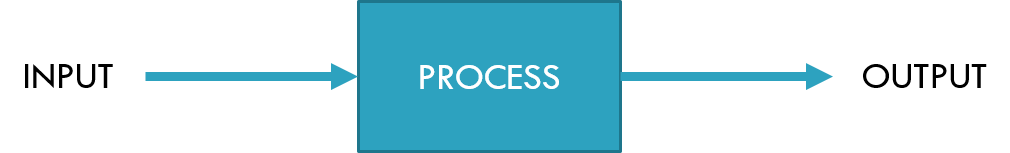
INTERCONNECTING THE SPM SYSTEM

**HOW IT ALL COMES TOGETHER.**

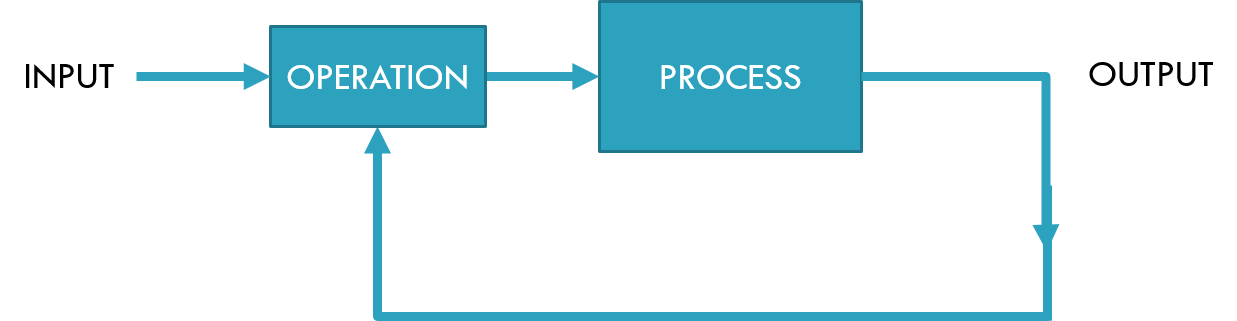
**The Diagram of the SPM**

First let us look at what is a block diagram for control systems looks like. A block diagram shows all the parts of an equipment. Certain diagrams also show the direction of the ‘flow’ meaning the order in which every part of the diagram contributes to the whole.

A simple block diagram looks like this:

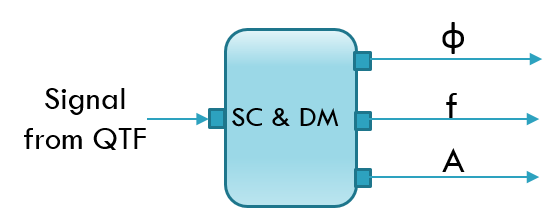


This is an open loop block diagram because the output is not connected to the input in any way. A closed loop block diagram looks like this.

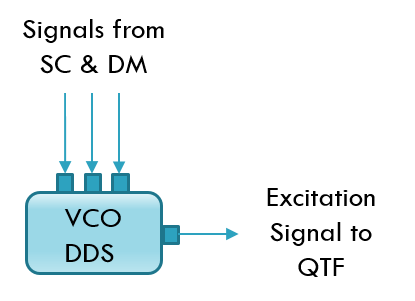


And the main difference is that the ouput signal is used to modify the input signal that goes into the ‘process’ block.

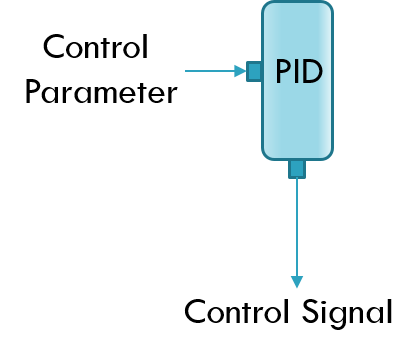
An SPM system is a more complicated closed loop, but the main characteristic are the same. A part of the block is used to demodulate the signal measured from the QTF. We call it here the Signal Conditioning and Demodulation module (SC&DM). Its output are the main parameters of the signal, namely Phase, Frequency and Amplitude.



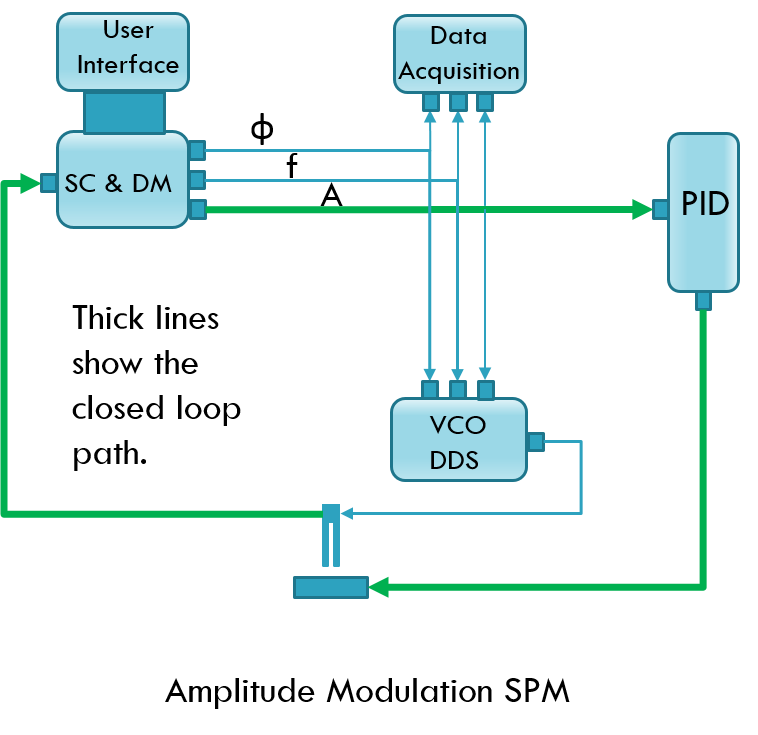
Another part is the signal generator. It receives the demodulated information from the SC&DM module and generates the signal that is used for excitation and also for synchronization.



Finally, the PID module that process the signal and tries to maintain the a Control Paremeter signal close to a pre-determined value (not shown). Its output is the part of the loop that controls the tip sample distance by sending a signal to the piezoelectric system. The output is called the Control Signal.

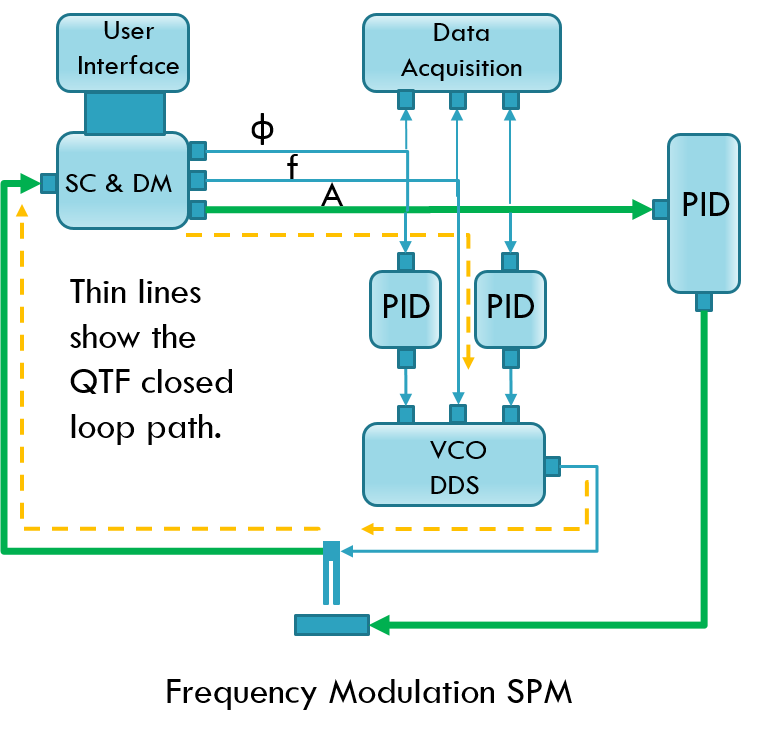


The whole diagram is shown in figure (). It also has the User interface and the Data acquisition parts. The thick lines show the path that encompasses the feedback loop of the SPM control.



The frequency modulation, as we will see, is a modification of the system described above with the purpose of increase the control over the parameters of the probe’s motion. In the AM scheme the amplitude is passively measured to feed the feedback system. In contrast the FM scheme seeks to control the oscillation of the probe itself by adding PID loops to the excitation loop, that has remained open in the AM diagram.

By adding a PID block in between the SC&DM block the closed loop for the QTF excitation is implemented. Figure () shows in dashed lines the path that corresponds to the excitation closed loop.



PART 3

HOW TO CONTROL THE SPM SYSTEM

The Scanning and Imaging software has ben developed in Labview. It communicates with the FPGA by sending the scanning parameters and receiving the data from the interactions. However only the data acquisition uses the DMA feature, to ensure that there is no interruption in the FPGA alghorithm.

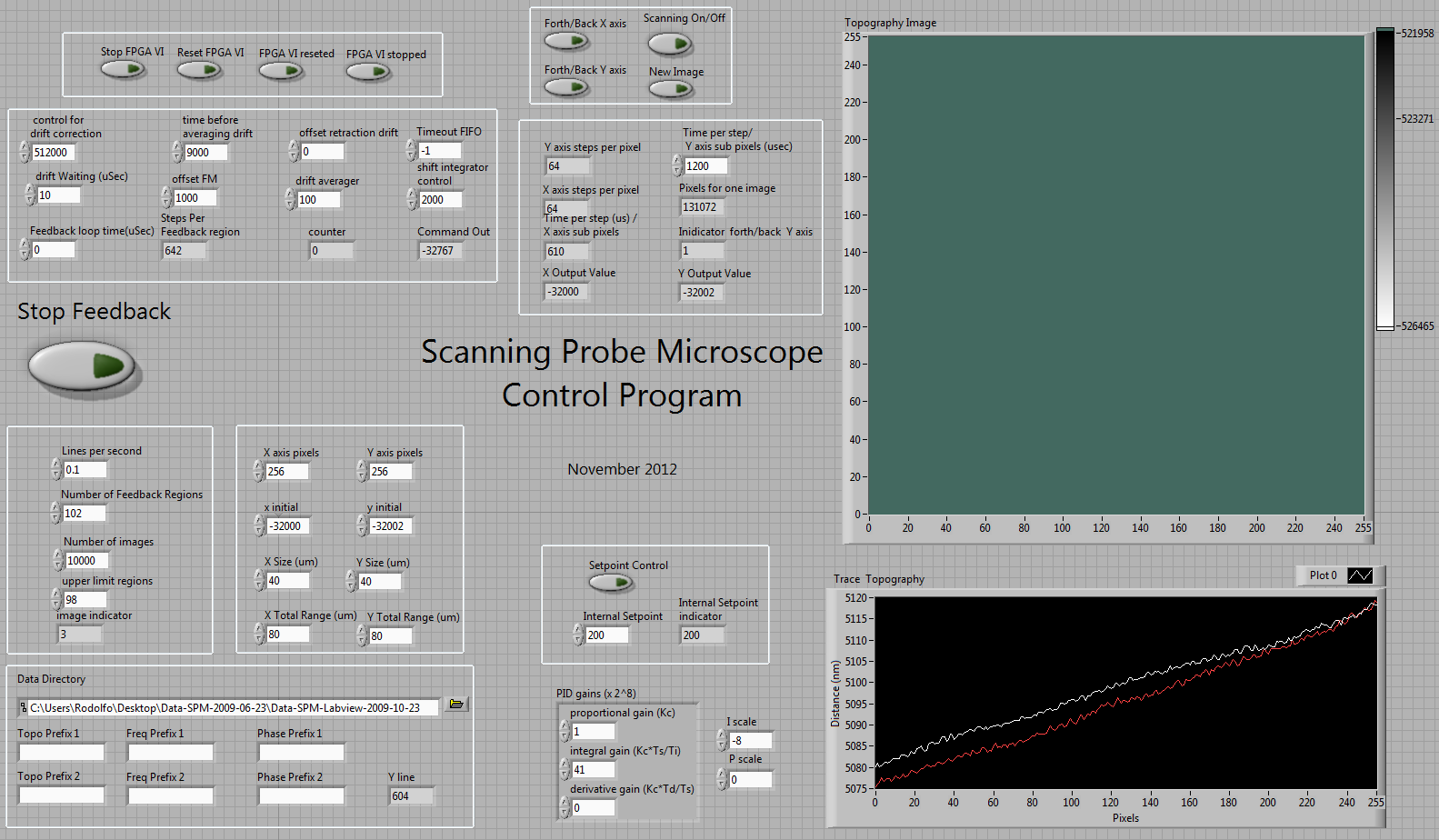
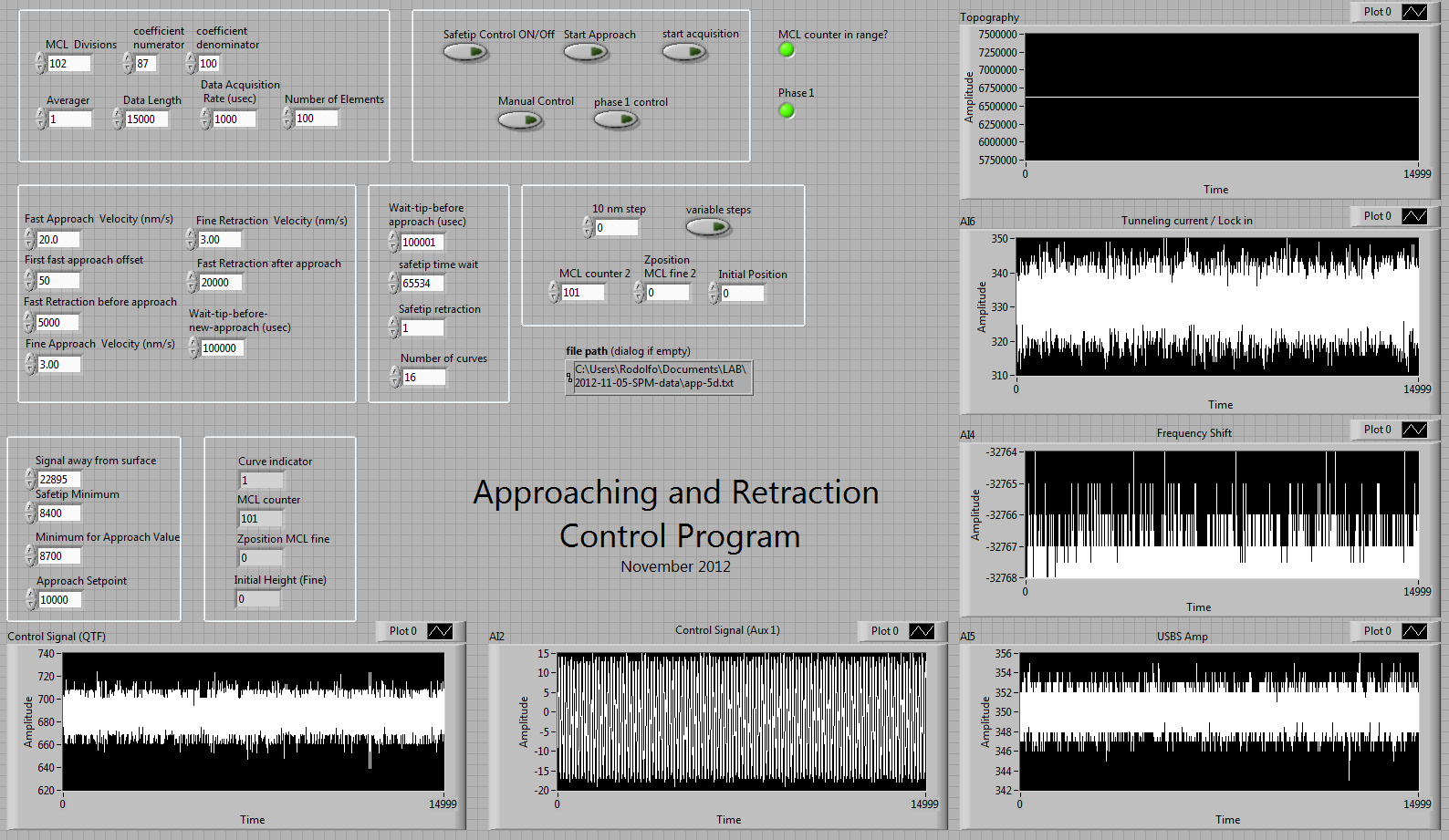
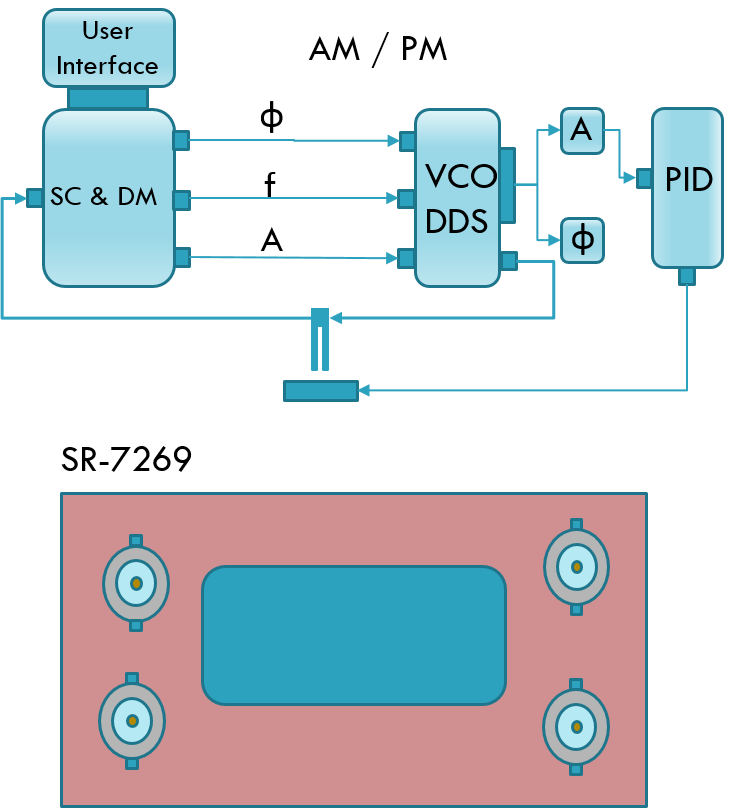
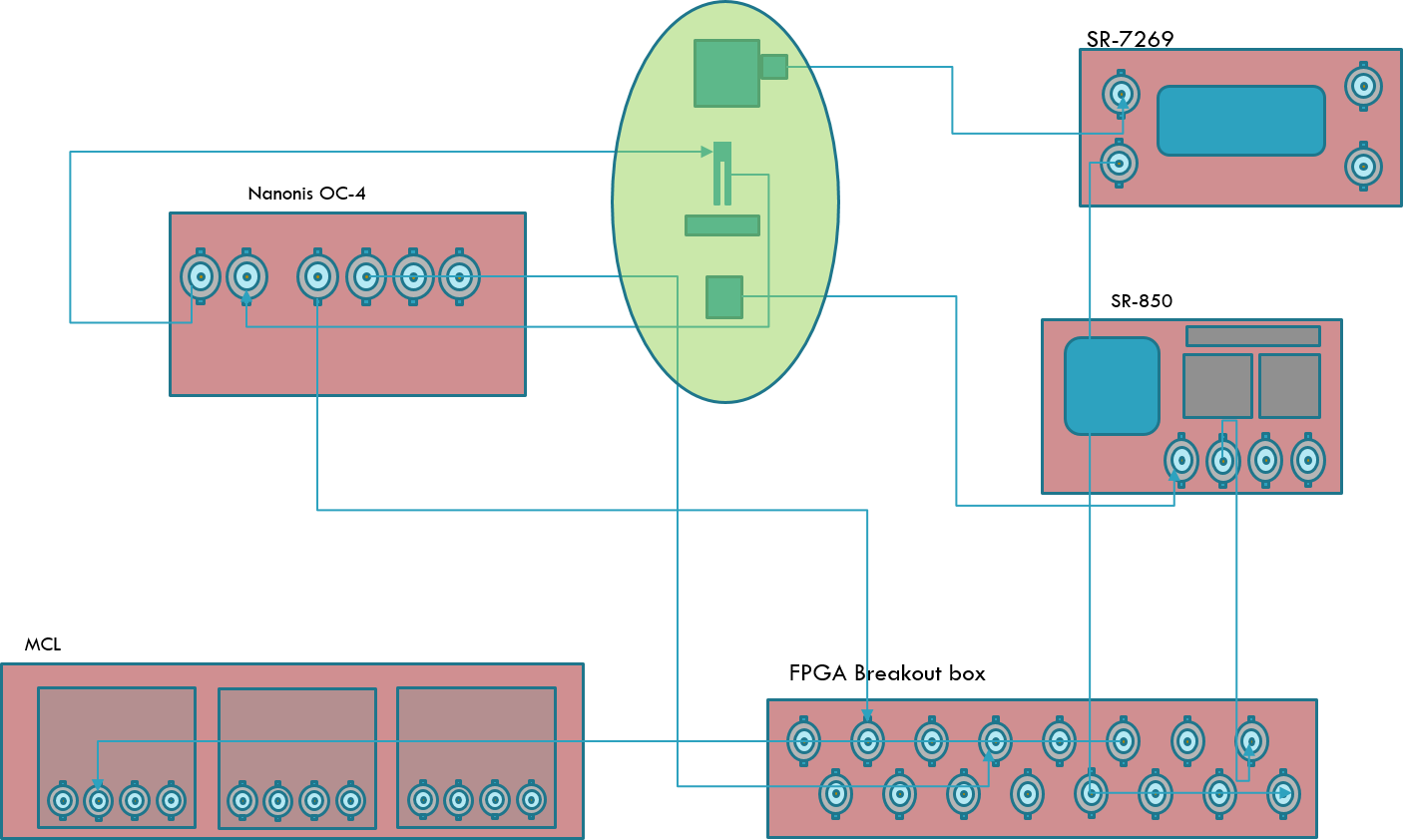


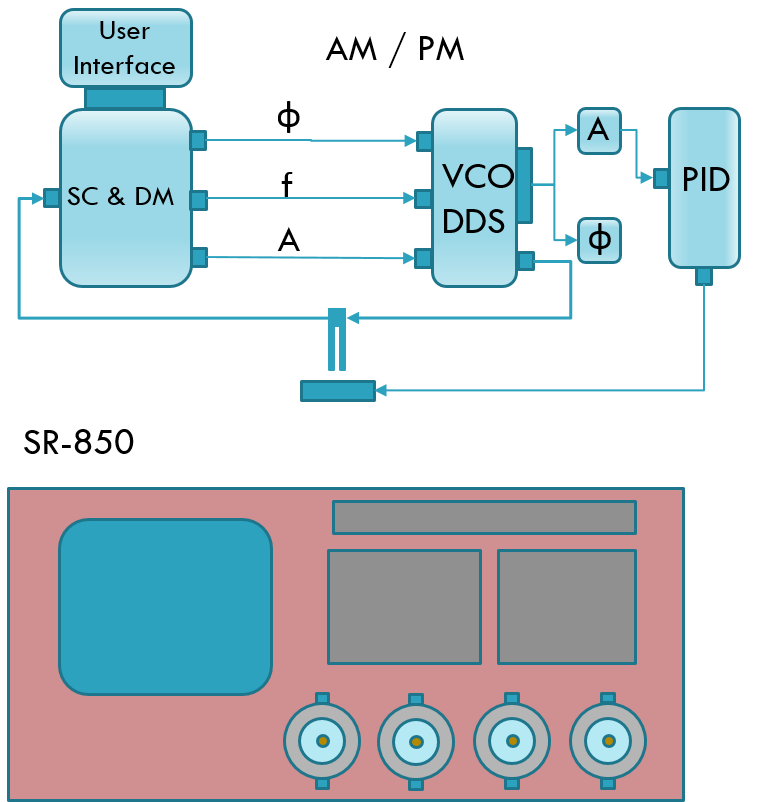
Figure () shows the GUI of the Scanning and Imaging software.



The SPM Head.







PART 4

EXAMPLES OF MEASUREMENTS.